AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

What is claimed is:

1. (Currently amended) An electronic substrate, comprising:

a substrate having two ~~one~~ or more electrically conductive inner layers; and

one or more interconnect cavities extending into, but not through, the substrate, each exposing two ~~one~~ or more of the two ~~one~~ or more electrically conductive inner layers.

2. (Currently amended) The electronic substrate of claim 1, wherein the substrate further comprises one or more electrically conductive surface layers, wherein one or more of the interconnect cavities extends from at least one of the one or more electrically conductive surface layers to at least one or more of the two ~~one~~ or more electrically conductive inner layers.

3. (Currently amended) The electronic substrate of claim 1, wherein at least one of one or more interconnect cavities comprises a base adjacent to one of the two ~~one~~ or more electrically conductive inner layers, the base comprising a layer of electrically conductive material.

4. (Currently amended) The electronic substrate of claim 1, wherein at least one of the one or more interconnect cavities comprises a base adjacent to one of the two ~~one~~ or more electrically conductive inner layers, wherein the interconnect cavity defines a wall interconnected with the base adjacent electrically conductive inner layer.

5. (Currently amended) The electronic substrate of claim 1, wherein at least one of the interconnect cavities comprises a base adjacent to and electrically interconnected with one of the two ~~one~~ or more electrically conductive inner layers, the interconnect cavity

extending from a surface layer defines a wall interconnected with the base adjacent electrically conductive inner layers and the surface layer.

6. (Previously presented) The electronic substrate of claim 1, wherein at least one of the interconnect cavities is adapted to receive and interconnect with electrically conductive interconnect material.

7. (Original) The electronic substrate of claim 1, wherein the interconnect cavities are positioned to correspond with land pads of a surface mount technology electrical component.

8. (Currently amended) The electronic substrate of claim 1, wherein at least one of the interconnect cavities comprises a base adjacent to one of the two ~~one~~ or more electrically conductive inner layers, and an opening at a surface of the substrate, the base having a smaller diameter than the opening.

9. (Withdrawn) The electronic substrate of claim 1, wherein each interconnect cavity comprises a base adjacent to one of the inner layers and an opening at a surface of the substrate, the base having a larger diameter than the opening.

10. (Withdrawn) A method for making a substrate for interconnecting electronic components comprising:

providing a substrate having one or more electrically conductive inner layers; and

forming a cavity extending from a surface of the substrate, the cavity exposing one or more inner layers.

11. (Withdrawn) The method of claim 10, wherein providing a substrate having one or more electrically conductive inner layers comprises providing a substrate having one or more electrically conductive inner layers and one or more electrically conductive surface layers; and wherein forming a cavity extending from the surface of the substrate, the cavity exposing one or more inner layer comprises forming a cavity extending from one of the surface layers to one or more inner layers.

12. (Withdrawn) The method of claim 11, further comprises depositing an electrically conductive material to form a liner in the cavity which is interconnected with the corresponding one or more inner layers and the surface layer.

13. (Withdrawn) The method of claim 12, wherein depositing an electrically conductive material comprises electroplating a layer of conductive material on walls of the cavity.

14. (Withdrawn) The method of claim 12, wherein depositing an electrically conductive material comprises using a vapor deposition process to form a layer of conductive material on the cavity walls.

15. (Withdrawn) The method of claim 10, wherein forming a cavity comprises using laser ablation.

16. (Withdrawn) The method of claim 10, wherein forming a cavity comprises using a resist mask and an etching process.

17. (Withdrawn) The method of claim 10, wherein forming a cavity comprises forming a cavity with a base having a smaller diameter than an opening at the surface of the substrate.

18. (Withdrawn) The method of claim 10, wherein forming a cavity comprises forming a cavity with a base having a larger diameter than and opening at the surface of the substrate.

19. (Currently amended) An electronic device comprising:

an electronic component having component interconnects; and

an electronic substrate interconnected with at least one of electronic components having:

a substrate including two ~~one~~ or more electrically conductive inner layers; and

one or more interconnect cavities extending into a surface of, but not through the substrate, each exposing two ~~one~~ or more of the two ~~one~~ or more electrically conductive inner layers.

20. (Currently amended) The electronic device of claim 19, wherein the substrate further comprises one or more electrically conductive surface layers, wherein one or more of the interconnect cavities extends from at least one of the surface layers to at least one or more of the two ~~one~~ or more electrically conductive inner layers.

21. (Previously presented) The electronic device of claim 19, wherein at least one of the interconnect cavities comprises a base adjacent to one of the electrically conductive inner layers, the base comprising a layer of electrically conductive material.

22. (Previously presented) The electronic device of claim 19, wherein at least one of the interconnect cavities comprises a base adjacent to one of the electrically conductive inner layers, wherein the interconnect cavity defines a wall interconnected with the base adjacent conductive inner layer.

23. (Original) The electronic device of claim 19, wherein the electronic component is a microelectronic die.